SPYROS TRAGOUDAS

School of Electrical, Computer, and Biomedical Engineering (ECBE)
Southern Illinois University Carbondale (SIUC), IL 62901
e-mail: spyros@siu.edu, work phone: (618) 453-7027

Professor, School of Electrical, Computer, & Biomedical Eng. (ECBE) (former ECE Dept.), SIUC (since 7/1/01).
- Director, School of ECBE (since 7/1/2020)
- Department Chair, ECE Department, SIUC (07/01/2012-6/30/2020).
- Director, NSF IUCRC Consortium for Embedded Systems, SIUC site (since 3/16/2009).

EDUCATION

- Ph.D., Computer Science, School of Engineering, University of Texas at Dallas, 1991.
- MS, Computer Science, School of Engineering, University of Texas at Dallas, 1988.
- Diploma (5-year degree with thesis), Computer Engineering, School of Eng., University of Patras, Greece, 1986

RESEARCH HIGHLIGHTS

Current research areas

- VLSI design & test: Neuromorphic architectures, threshold logic, designs with emerging devices.
- Hardware security: Trojan detection/prevention, counterfeit identification, and watermarking.
- Embedded systems & architectures: Functional safety and reliability.
- Deep learning: Architectures, accelerators, and applications.

Summary of accomplishments

- 94 peer-reviewed journals, 206 papers in conferences, 7 book chapters, 5 best paper awards
- PI and fiscal officer in 46 externally funded research grants that exceed $6.75 M
- 10 equipment/software donations
- 5 patents
- 6 keynotes/distinguished lectures and 64 invited presentations to universities/industries
- Outstanding Scholar Award, College of Engineering, SIUC (2004).

GRADUATE STUDENT SUPERVISION

30 doctoral dissertations, 79 MS-theses, 17 undergraduates supported by NSF REU

TEACHING EXPERIENCE

Courses in the areas of: Electronic Design Automation, VLSI Design, Computer Architecture, Hardware Testing/Security/Verification/Validation, Networks, Parallel/distributed computing, Digital design, Algorithms, Programming languages.

SERVICE HIGHLIGHTS

Chair of the Graduate Council at SIUC (2007-2008)

Editorial boards

- IEEE Transactions on Computers (since July 2021, 2007 to 2012)
- IEEE Transactions on Nanotechnology (2019, guest editor)
- VLSI Design (1997- 1999, 2007 to 2018)

- Research Letters in Electronics (2008 to 2009)
- Journal of Electrical and Computer Engineering (2010 to 2020)
- Journal of Universal Computer Science (1995 to date)
- ISRN Electronics (2011 to 2018)

Program/General Chair in IEEE International Conferences: 3

NSF panels: 6

CURRENT PROFESSIONAL AFFILIATIONS

IEEE-senior member (since 1987), ECEDHA (since 2013)

RECENT PUBLICATIONS (since 2010)

Peer-reviewed journal publications - *Advisees at time of research are denoted in italics*

1. *K. Gnawali,* S. Tragoudas, High-Speed Memristive Ternary Content Addressable Memory, IEEE Transactions on Emerging Topics in Computing (TETC), to appear.
2. *K. Gnawali,* S. Tragoudas, and H. Quinn, Developing Benchmarks for Radiation Testing of Microcontroller Arithmetic Units using ATPG, IEEE Transactions on Nuclear Science (TNS), vol. 68, no. 5. pp. 857-864, May 2021.
3. *K. Gnawali,* H. Quinn, and S. Tragoudas, Updates on Testing Microprocessors Effectively, IEEE Transactions on Nuclear Science (TNS), vol. 68, no. 5, pp.842-849, May 2021.
4. *A. Watkins* and S. Tragoudas, Radiation Hardened Latch Designs for Double and Triple Node Upsets, IEEE Trans. on Emerging Topics in Computing (TETC), vol. 8, no. 3, pp. 616-626, July-September 2020.
5. *P.K. Javvaji* and S. Tragoudas, Test pattern Generation and Critical Path Selection in the Presence of Statistical Delays, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), pp. 163-173, vol. 28, no.1, January 2020.
6. *K. P. Gnawali, B.R. Paudel,* and S. Tragoudas, Reliability Enhancements in Memristive Neural Network Architectures, IEEE Transactions on Nanotechnology (TNANO), vol. 18, pp.866-878, August 2019.
7. *P.K. Javvaji* and S. Tragoudas, On the Sensitization Probability of a Critical Path Considering Process Variations and Path Correlations, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), pp. 1196-1205, vol. 27, issue.5. May 2019.
8. *K. P. Gnawali, S. N. Mozaffari,* and S. Tragoudas, Low Power Spintronic Ternary Content Addressable Memory, IEEE Transactions on Nanotechnology (TNANO), pp. 1206-1216, vol. 17, no. 6, Nov. 2018.
9. *K. P. Gnawali, S. N. Mozaffari,* and S. Tragoudas, Low Power Artificial Neural Network Architectures, IEEE VLSI Circuits and Systems Letter, pp. 0-5, vol.4. issue 4, Nov. 2018, https://arxiv.org/pdf/1904.02183.pdf
10. *S. N. Mozaffari* and S. Tragoudas, Maximizing the number of threshold logic functions using resistive memory, IEEE Transactions on Nanotechnology (TNANO), pp. 897-905, vol. 12, no. 5. September 2018.
11. *S. N. Mozaffari*, S. Tragoudas, and Th. Haniotakis, A generalized approach to implement efficient CMOS-based threshold logic functions, IEEE Trans. on Circuits and Systems I (TCAS-I), pp. 946-.959, vol.65, no.3. Mar. 2018
12. S. Leitner, H. Wang and S. Tragoudas, Design of Scalable Hardware-Efficient Compressive Sensing Image Sensors, IEEE Sensors journal, pp.641-651, vol. 18, no.2. January 2018.
13. *S. N. Mozaffari*, S. Tragoudas, and Th. Haniotakis, More Efficient Testing of Metal-oxide Memristor-based Memory, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 36, no. 6, pp. 1018- 1029, June 2017.
14. *C.B. Dara*, Th. Haniotakis, and S. Tragoudas, Delay Analysis for Current Mode Threshold Logic Gate Designs, IEEE Trans. on Very Large Scale Integration Systems (TVLSI), vol. 25, no. 3, pp. 1063- 1071, March 2017.

15. S. Leitner, H. Wang, and S. Tragoudas, Design Techniques for Direct Digital Synthesis with Improved Frequency Accuracy over Wide Frequency Ranges, Journal of Circuits, Systems and Computers, Elsevier, (21 pages), vol. 26, issue 2, February 2017.
16. *A. M. Somashekar* and S. Tragoudas, Diagnosis of Performance Limiting Segments in Integrated Circuits using Path Delay Measurements, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), pp. 325-335, vol. 36., no. 2, February 2017.
17. *A. M. Somashekar*, S. Tragoudas, R. Jayabharathi, and *S. Gangadhar*, Non-enumerative Generation of Path Delay Distributions and its Application to Critical Path Selection, ACM Transactions on Design Automation of Electronic Systems (TODAES), pp.17:1-17:21, vol. 22, issue 1, article 17, Dec. 2016.
18. *A. K. Palaniswamy*, S. Tragoudas, and Th. Haniotakis, ATPG for Delay Defects in Current Mode Threshold Logic Circuits, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), pp. 1903 – 1913, vol. 35, no. 11, November 2016.
19. *S. Mohanty* and S. Tragoudas, Scalable Off - Line Searches in DNA sequences, ACM Journal on Emerging Technologies in Computing (JETC), pp. 18:1 – 18:25, vol. 11, issue 2, November 2014.
20. *J. Lenox* and S. Tragoudas, Adapting an Implicit Path Delay Grading Method for Parallel Architectures, IEEE Trans. Computer-Aided Design of Int. Circuits and Systems (TCAD), pp. 1965 - 1976, vol. 33, no. 12, Dec. 2014.
21. *K. Karmakar* and S. Tragoudas, Error Correction Encoding for Tightly Coupled On-Chip Buses, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), pp. 2571-2584, vol. 22, no. 12, December 2014.
22. *A.K. Palaniswamy* and S.Tragoudas, Improved threshold logic synthesis using implicant-implicit algorithms, ACM Journal on Emerging Technologies in Computing (JETC), pp. 21:1- 21:32, vol. 10, issue 3, April 2014.
23. *K. Karmakar* and S. Tragoudas, On-Chip Codeword Generation to Cope with Crosstalk, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, no. 2, pp 237-250, Feb. 2014.
24. *L. Pierce* and S. Tragoudas, Nanopipelined Threshold Network Synthesis, ACM Journal on Emerging Technologies in Computing (JETC), vol. 10, no. 2, pp. 17:1-17:17, February 2014.
25. *S. Gangadhar* and S. Tragoudas, A Probabilistic Approach to Diagnose SETs in Sequential Circuits, Journal of Electronic Testing: Theory and Applications (JETTA), vol. 29, pp. 317-330, March 2013.
26. *L. Pierce* and S. Tragoudas, Enhanced Secure Architecture for JTAG Systems, IEEE Transactions on Very Large Scale Integration Systems (TVLSI), vol. 21, no. 7, pp. 1342-1345, July 2013.
27. *A.K. Palaniswamy* and S.Tragoudas, An Efficient Heuristic to Identify Threshold Logic Functions, ACM Journal on Emerging Technologies in Computing (JETC), pp.19:1-19:17, vol. 8, is. 3, Aug. 2012.
28. *M.N. Skoufis*, S. Tragoudas, An on-line Failure Detection Method for Data Buses using Multi-threshold Receiving Logic, IEEE Transactions on Computers (TC), vol. 61, no. 2, pp. 187-198, Feb. 2012
29. *K.J. Stewart*, Th. Haniotakis, and S. Tragoudas, Securing sensor networks: A Novel Approach that Combines Encoding, Uncorrelation, and Node Disjoint Transmission, Ad Hoc Networks, vol.10, iss.3, pp. 328-328, 2012.
30. *R. Adapa*, S. Tragoudas, and M.K. Michael, Improved Diagnosis Using Enhanced Fault Dominance, Integration, the VLSI journal, vol. 44, issue 3, pp. 217-228, June 2011.
31. *M.N. Skoufis, K. Karmakar*, S. Tragoudas, and T. Haniotakis, A data capturing method for buses on chip, IEEE Transactions on Circuits and Systems I (TCAS-I), vol. 57, no. 7, pp.1631-1641, July 2010.
32. D*. Jayaraman*, R. Sethuram, and S. Tragoudas, Scan Shift Power Reduction by Gating Internal Nodes. Journal of Low Power Electronics (JLPE), 6(2): 311-319 (2010).
33. *E. Flanigan*, S. Tragoudas, Path Delay Measurement Techniques using Linear Dependency Relationships, IEEE Transactions on VLSI Systems (TVLSI), vol. 18, no. 6, pp.1011-1015, June 2010.
34. *R. Adapa*, S. Tragoudas, Techniques to Prioritize Paths for Diagnosis, IEEE Transactions on VLSI Systems (TVLSI), vol. 18, issue 4, pp. 658-661, April 2010.

Publications in peer reviewed conference proceedings - *Advisees at time of research in italics*

1. *B.R. Paudel, H.B.M. Senarathna,* H. Wang*,* S.Tragoudas*,* Y. Hu, and S. Jiang, Predicting YOLO Misdetection by Learning Grid Cell Consensus, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.
2. *V. Pentsos, B.R. Paudel,* S.Tragoudas, K.N. Gowda, and M. Schmit, Improved CNN Classification Accuracy with the Addition of Shallow Cascading CNNs, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.

3. *B.R. Paudel, A. Itani,* and S.Tragoudas, Adversarial Robustness Assessment and Defense in SNN against Black Box Attacks, Proceedings of the 20th IEEE International Conference on Machine Learning and Applications (ICMLA), December 13-16, 2021, Pasadena, CA.
4. *P. Savanur* and S.Tragoudas*,* A Fault Model to Detect Design Errors in Combinational Circuits, Proceedings of the 34th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 6-8, 2021, Athens, Greece (virtual).
5. *B. Shanyour,* and S. Tragoudas, Broadside ATPG for Low Power Trojans Detection using Built-in Current Sensors, Proceedings of the 26th IEE International Symposium on On-Line, Testing and Robust System Design, July 13-15, 2020, Naples, Italy.
6. *K. Gnawali,* S. Tragoudas, and H. Quinn, Updates on Testing Microprocessors Effectively, Proceedings of the 2020 Nuclear and Space Radiation Effects Conference (NSREC), July 20-24, 2020, Santa Fe, NM.
7. *K. Gnawali,* H. Quinn, and S. Tragoudas, Developing Benchmarks for Radiation Testing of Microcontroller Arithmetic Units using ATPG, Proceedings of the 2020 Nuclear and Space Radiation Effects Conference (NSREC), July 20-24, 2020, Santa Fe.
8. *B. Shanyour,* S. Tragoudas, Detection of Low Power Trojans in Standard Cell Designs using Built-In Current Sensors, Proceedings of the 2018 International Test Conference (ITC), October 28- November 2, 2018, Phoenix, AZ.
9. *S.N. Mozaffari, K.P. Gnawali,* and S. Tragoudas, An aging resilient neural network architecture, Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), July 2018, Athens, Greece.
10. *P. Javvaji,* S. Tragoudas, A method to model statistical path delays for accurate defect coverage, Proceedings of the 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 8-10, 2018, Chicago, IL
11. *P. Savanur,* S. Tragoudas, Threshold Voltage Extraction using NBTI aging, Proceedings of the 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), October 8-10, 2018, Chicago, IL
12. *P. Javvaji,* S. Tragoudas, and G. Kondapuram*,* Scalable fault coverage estimation in sequential circuits without fault injection, Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), May 27-30, 2018, Florence, Italy.
13. *P. Javajji*, *B. Sanyour* and S. Tragoudas, Test set identification for improved delay coverage in the presence of statistical delays, Proceedings of the 2018 IEEE International Symposium on Quality of Electronic Design (ISQED), March 13-14, 2018, Santa Clara, CA.
14. *P. Savanur* and S. Tragoudas, A method to determine the static NBTI stress time of an embedded component in an integrated circuit, Proceedings of the International Conference on Advances in System Testing and Validation Lifecycle (VALID) Conference, October 8-12, 2017, Athens Greece. (Best paper award.)
15. *Th. Toulas* and S. Tragoudas, Diagnosis with Transition Faults on Embedded Segments, Proceedings of the IEEE International On-Line Test Symposium (IOLTS), July 3 - 6, 2017, Thessaloniki, Greece.
16. *A. M. Somashekar* and S. Tragoudas, Efficient Critical Path Selection under a Probabilistic Delay Fault Model, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2017, to appear.
17. *A. Watkins* and S. Tragoudas, METS: A Multiple Event Transient Simulator, Proceedings of the 2017 IEEE International Symposium on Circuits and Systems (ISCAS), May 2017, Baltimore, MD.
18. *P.K. Javvaji* and S. Tragoudas, Efficient Computation of the Sensitization Probability of a Critical Path considering Process Variations and Path Correlation, Proceedings of the 2017 IEEE International Symposium on Circuits and Systems (ISCAS), May 2017, Baltimore, MD.
19. *S.N. Mozaffari*, S. Tragoudas, Th. Haniotakis, Reducing power, area and delay of threshold logic gates considering non-integer weights, Proceedings of the 2017 IEEE International Symposium on Circuits and Systems (ISCAS), May 2017, Baltimore, MD.
20. *S.N. Mozaffari* and S. Tragoudas, Memristive Current Mode Threshold Logic Gates, Proc. of the 1st International Conference on Memristive Materials, Devices and Systems (MERISYS 2017), April 3-6, 2017, Athens, GR.
21. *S.N. Mozaffari*, S. Tragoudas, Th. Haniotakis, A new method to identify threshold logic functions, Proceedings of the 20th Design Automation and Test in Europe (DATE) Conference, March 27 – 31, 2017, Lausanne, CH.

22. *Ph. Alladi* and S. Tragoudas, Aging-aware critical paths for process related validation in the presence of NBTI, Proceedings of the IEEE International Symposium on Quality of Electronic Design (ISQED), March 13 - 17, 2017, Santa Clara, CA
23. *A. Watkins* and S. Tragoudas, A Highly Robust Double Node Upset Tolerant Latch, Proceedings of the 29th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), September 19-20, 2016, Stores, CT.
24. S. Leitner, H. Wang, and S. Tragoudas, Compressive Image Sensor Technique with Sparse Measurement Matrix, 29th IEEE International System-on-Chip Conference (SOCC), September 6-9, 2016, Seattle, WA.
25. *W. Al Jubouri*, S. Tragoudas, Th. Haniotakis, Identification of delay defects on embedded paths using one current sensor, Proceedings of the 11th IEEE International Conference on Design and Technology of Integrated Systems in nanoscale era (DTIS), April 12-14, 2016, Instabul, Turkey.
26. *Ph. Alladi* and S. Tragoudas, Efficient Selection of critical paths for delay defects in the presence of process variations, Proceedings of the 11th IEEE International Conference on Design and Technology of Integrated Systems in nanoscale era (DTIS), April 12-14, 2016, Instabul, Turkey.
27. *A. Watkins* and S. Tragoudas, An Enhanced Analytical Electrical Masking Model for Multiple Event Transients, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 99-104, May 2016, Boston, MA.
28. *A. M. Somashekhar*, S. Tragoudas, and R. Jayabharathi, Non-Enumerative Correlation-Aware Path Selection, Proceedings of the 33rd International Conference on Computer Design (ICCD), pp. 629-633, October 2015, New York City, NY
29. *P.R. Savanur, Ph. Alladi,* and S. Tragoudas, A BIST Approach for Counterfeit Circuit Detection based on NBTI Degradation, Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 123-126, Oct. 12-14, 2015.
30. *S. N. Mozaffari,* S. Tragoudas, and Th. Haniotakis, Fast March Tests for Defects in Resistive Memory, Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), July 8-10, 2015, Boston, MA, USA.
31. *J. Lenox* and S. Tragoudas, Towards Trojan Circuit Detection with Maximum State Transition Exploration, Proceedings of the IEEE International On-Line Test Symposium (IOLTS), July 6-8, 2015, Elia, Halkidiki, Greece.
32. *L. Piece* and S. Tragoudas, Unreachable Code Identification for Improved Line Coverage, Proceedings of the 2015 IEEE International Symposium on Quality of Electronic Design (ISQED), March 2-4, 2015, Santa Clara, CA.
33. *W. Al Jubouri*, A. M. Somashekar, Th. Haniotakis, S. Tragoudas, Identification of segment delay defects with current sensing, Proceedings of the IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 122-127, October 2014.
34. *P. Alladi*, S. Tragoudas, Aging-aware Critical Paths in Deep Submicron, Proceedings of the IEEE International On-Line Test Symposium, Platja d'Aro, Catalunya, Spain (IOLTS), July 7-9, 2014.
35. *A. Palaniswamy*, S. Tragoudas, T. Haniotakis, ATPG for Transition Faults of Pipelined Threshold Logic Circuits, Proceedings of the 9th IEEE International Conference on Design and Technology of Integrated Systems in nanoscale era (DTIS), 6-8 May 2014, Santorini, Greece
36. *J. Lenox* and S. Tragoudas, A novel parallel adaptation of an implicit path delay grading method, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), May 2014, Houston Texas.
37. *A. Watkins*, V.N. Mudhireddy, H. Wang and S. Tragoudas, Adaptive Compressive Sensing for Low Power Wireless Sensors, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 99-104, May 2014, Houston Texas.
38. K. *Karmakar* and S. Tragoudas, Error Detection Encoding for Multi-threshold Capture Mechanism. Proceedings of the IEEE International On-Line Test Symposium (IOLTS), July 7-9, 2013 Chania, Greece
39. *D. Jayaraman* and Spyros Tragoudas, Performance Validation Through Implicit Removal of Infeasible Paths of the Behavioral Description, Proceedings of the 2013 IEEE International Symposium on Quality of Electronic Design (ISQED), March 5 - 6, 2013, Santa Clara, CA
40. *A. Mysore Somashekar* and Spyros Tragoudas, Diagnosis of Small Delay Defects Arising Due to Manufacturing Imperfections Using Path Delay Measurements, Proceedings of the 2013 IEEE International Symposium on Quality of Electronic Design (ISQED), March 5-6, 2013, Santa Clara, CA
41. *D. Jayaraman* and Spyros Tragoudas, A Method to Determine the Sensitization Probability of a Non-Robustly Testable Path, Proceedings of the 2013 IEEE International Symposium on Quality of Electronic Design (ISQED), March5-6, Santa Clara, CA

42. *C. B. Dara*, T. Haniotakis, S. Tragoudas, "Low power and high-speed current-mode memristor-based threshold logic gates," Proc. IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp.89-94, Oct. 2013.
43. *C. B. Dara*, T. Haniotakis, S. Tragoudas, "Delay Analysis for an N-Input Current Mode Threshold Logic Gate," Proc. International Symposium on VLSI (ISVLSI), pp. 344-349, 2012
44. *A. Watkins* and S. Tragoudas, Transient Pulse Propagation Using the Weibull Distribution Function, Proceedings of the 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS 2012), 1-3 October 2012, Austin, TX.
45. *A.M. Somashekhar*, *S. Gangadhar*, S. Tragoudas and R. Jayabharathi, Non-enumerative generation of statistical path delays for ATPG, Proceedings of the International Conference of Computer Design (ICCD), Sept. 30-Oct.3 2012.
46. *A.K. Palaniswamy* and S.Tragoudas, A scalable threshold logic synthesis method using ZBDDs, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI),pp. 307-310, May 3-4, 2012, Salt Lake City, UT.
47. *S. Gangadhar* and S. Tragoudas, Accurate calculation of SET probability for hardening, Proceedings of the 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 1-3 October 2012, Austin, TX.
48. *A.M. Somashekhar*, S. Gangadhar, S. Tragoudas and R. Jayabharathi, Non-enumerative generation of statistical path delays for ATPG, Proceedings of the International Conf. of Computer Design (ICCD), Sept. 30-Oct.3 2012.
49. *A.K. Palaniswamy* and S.Tragoudas, A scalable threshold logic synthesis method using ZBDDs, Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI),pp. 307-310, May 3-4, 2012, Salt Lake City, UT.
50. *P. Alladi, P.P. Mohanty* and S. Tragoudas, A scalable method for arbitrary string searches in DNA sequence, Proceedings of the ISCA 4th International Conference on Bioinformatics and Computational Biology (BICoB), March 12-14, 2012, Las Vegas, Nevada, USA.
51. *L. Pierce* and S. Tragoudas, Multi-level secure JTAG architecture, Proceedings of the 17th IEEE International On-Line Testing Symposium (IOLTS), pp. 208-209, 13-15 July 2011.
52. *S. Gangadhar*, S. Tragoudas, An analytical method for estimating SET propagation, Proceedings of the 29th VLSI Test Symposium (VTS), pp. 197-202, 2011
53. *S. Gangadhar,* and S. Tragoudas, A probabilistic Approach to Diagnose SETs, Proceedings of the 2011 IEEE Int. Symp. on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 261-267, 3-5 Oct. 2011.
54. *K. Karmarkar* and S. Tragoudas, Error correction encoding for multi-threshold capture mechanism, Proceedings of the 17th IEEE International On-Line Test Symposium, (IOLTS), pp. 157-162, 13-15 July 2011.
55. *C.B. Dara,* S. Tragoudas, and T. Haniotakis. A Metric for Weight Assignment to Optimize the Performance of MOBILE Threshold Logic Gate, In Proc. IEEE International Symposium on Defect and Fault tolerance in VLSI and Nanotechnology (DFT), pp. 131-138, Oct. 2011.
56. *P.P. Mohanty*, and S. Tragoudas. A scalable method for identifying DNA substrings using functions, Proceedings of the 3rd International Conf. on Bioinformatics and Computational Biology (BICOB), pp. 178-183, March 2011.
57. *D. Jayaraman*, and S. Tragoudas. Occurrence probability analysis of a path at the architectural level, Proceedings of the IEEE International Symposium on the Quality of Electronic Design (ISQED), pp. 464-468, March 2011.
58. *K. Karmakar*, S. Tragoudas, Scalable codeword generation for coupled buses, Proceedings of the 13th Design Automation and Test in Europe (DATE) Conference, pp. 729-735, 8-12, March 2010, Dresden, Germany.
59. *S. Gangadhar*, S. Tragoudas, A Novel Probabilistic SET Propagation Method, in Proceedings of the 10th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 258-263, March 2010.
60. *D. Jayaraman*, R. Sethuram, and S. Tragoudas, Gating internal nodes to reduce power during scan shift, Proc. of the 2010 ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 79-84, October 2010.
61. *S. Gangadhar*, S. Tragoudas, Probabilistic methods for the impact of an SET in combinational logic, Proceedings of the 16th IEEE International Online Testing Symposium (IOLTS), pp.41-46, July 2010.
62. *M.N. Skoufis*, S. Tragoudas, On-line Detection of Random Voltage Perturbations in Buses with Multiple-threshold Receivers, Proceedings of the 16th IEEE International Online Testing Symposium (IOLTS), pp.249-254, July 2010.
63. *A.K. Palaniswamy, M.K. Goparaju*, S. Tragoudas, Scalable identification of threshold logic functions, Proc. of the 2010 ACM Great Lakes Symposium on VLSI (GLSVLSI), pp. 269-274, October 2010.